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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,713	11/01/2001	Michael E. Ichiriu	N1-P107	3008

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,713	ICHIRIU ET AL.	
	Examiner	Art Unit	
	JAMES C KERVEROS	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-61* is/are pending in the application.

4a) Of the above claim(s) *23-38 and 50-61* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22 and 39-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is a Final Office Action in response to Amendment filed August 2, 2004, in reply to the Office Action mailed April 6, 2004.

2. Claims 23-38 and 50-61 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant's election without traverse of claims 1-22 and 39-49 in the reply filed on August 2, 2004 is acknowledged.

3. Claims 1-61 are pending and claims 22 and 39-49 are presently under examination.

4. Prior Office Action Objections to the Claims and Drawings are hereby withdrawn, in view of amendment to the claims and formal drawings enclosed.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-21, 39-44 and 46-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh et al. (US 6625766).

Regarding Claims 1, 2, 39 and 44, Oh substantially discloses an apparatus and method for testing a semiconductor memory device, comprising:

A CAM, such as a semiconductor memory array (100), which has a plurality of rows of cells.

FIG. 6 shows an address generating circuit with identical upper and lower portions relating to X and Y address, respectively. For examination purpose only the upper portion X address generation circuit will be taken into consideration.

A first counter circuit including an X-address minimum value register (40) and an (address counter 44) coupled to the memory array (100) and adapted to store an address value from X-address minimum value register 40 in response to a load signal, and to incrementally adjust the address value in response to a first control signal (XCLK) and to further reset the address value for a start address in response to a second control signal (CLEAR).

A second counter circuit including an X-address maximum value register (42) for storing a limit value (X-maximum value).

A compare circuit (60) coupled for receiving the address value from the first counter circuit (44) and the limit value from the second counter circuit (42), where the compare circuit (60) generates the second control signal (CLEAR) same as X carry out signal XCARRY, if the address value (44-OUT) and the limit value (42-OUT) have the same value, then XCARRY is logic "1".

Regarding Claims 39 and 44, in addition to the common limitations applied to claim 1 above, Oh further discloses means (address counter 44) for accessing data stored at a first address value (minimum value Xmin) in the semiconductor memory array (100), in response to (CLEAR) and clock signals XCLK and an address decoder, which is normally coupled between the first counter (44) and the memory array (100) for selecting one of the rows (X-address) of memory cells corresponding to the address.

Regarding independent Claims 1, 39, 44, and dependent 3, 11, 17 and 18, Oh does not disclose a second counter for incrementally adjusting the limit value in response to the second control signal. However, Oh discloses substantially an identical counter circuit including an X-address minimum value register (40) and (address counter 44) coupled to the memory array (100). Further, he discloses a second counter circuit including an X-address maximum value register (42). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to add the identical address counter 44 between the register (42) and the comparison circuit 60, in the second counter circuit of Oh, as to incrementally adjust the limit value by increasing or decreasing the counter accordingly, in response to the second control signal (CLEAR), since the counter in the second counter circuit functions identically with the counter in the first counter circuit.

Regarding Claims 4-6, Oh discloses first counter (X address counter 44), which increases by one up to 1023, in response to the clock signal XCLK, wherein the counter

incrementally adjusts the address value by decreasing the address value by a count of one.

Regarding Claims 7-9, 12-15 and 40-43, Oh discloses address counter 44, which inputs a minimum value Xmin, in response to a load signal (LOAD), corresponding to a storage location in memory array (100) and increasingly counting in response to clock signals XCLK, starting from the minimum value Xmin and reaching the maximum value, Xmax, of X addresses, and where the Xmin and Xmax value can represent the starting address of the memory.

Regarding Claims 10 and 6, Oh discloses a programmable storage elements registers (40) and (42), which store X address minimum value (Xmin) and X address maximum value (Xmax), respectively, representing the starting address of the memory.

Regarding Claims 19-21 and 46-49, Oh does not disclose a third counter circuit to store a block select value, the third counter being adapted to incrementally adjust the block select value in response to a third control signal and to assert the first control signal when the block select value reaches a predetermined value, and further a fourth counter circuit to store a block select limit and to incrementally adjust the block select limit in response to the fourth control signal, and a block select compare circuit coupled to receive the block select value from the third counter circuit and the block select limit from the fourth counter circuit, the block select compare circuit being adapted to assert the fourth control signal if the block select value and the block select limit have a predetermined relationship.

However, Oh substantially discloses an address generator comprising a first counter circuit, which includes an X-address minimum value register (40) and an (address counter 44) and a second counter circuit having an X-address maximum value register (42) for generating an X, Y address for selecting memory locations. The disclosed address generator similarly is capable of adjusting a storage memory block select value. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use identical counters, as taught by Oh, for the purpose of selecting storage memory blocks, since the disclosed address counters perform memory cell as well as storage block selection.

7. Claims 22 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh et al. (US 6625766) in view of Giles et al. (US 6085334).

Regarding Claim 22, 45, Oh substantially discloses a semiconductor memory array (100) including a plurality of rows of cells and a plurality of word lines (data lines) coupled respectively to the plurality of rows of cells, as shown by an address generating circuit 22 and a data generating circuit 24, in the prior art, FIG. 2.

An address decoder coupled between the plurality of word lines and the address value (XA0, XA1, XA2,.....XA16) generated from the first counter circuit, (44, FIGS. 6 and 7), where the address decoder activates one of the plurality of word lines (DATA) according to the address value (X,Y) such that the data word is coupled to the output of the memory array (100).

Oh does not disclose an error detector coupled to receive the data word from a CAM array and having circuitry to determine whether the data word contains an error. Howe ver, Giles et al. (US 6085334) discloses a built-in self-test (BIST) and self-repair of memory (BISR) devices, including an error detector data compare 34,which receives the data word output from the CAM array (40), verifies the memory output data at the address under test and determines whether the data word contains an error. When an error is detected, data compare 34 provides a fail indication to error qualifier 38, which provides a repair signal to BISR circuit 39 including a content addressable memory (CAM), FIG. 1. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to add an error detector, as taught by Giles, at the output data of the memory array of Oh, for the purpose of detecting memory device defects, which are sensitive to environmental conditions and are not exhibited over the entire operating range of the device, as to assure the quality and proper operation of the memory device.

Response to Arguments

8. Applicant's arguments filed August 2, 2004 have been fully considered but they are not persuasive. Claims 1-21, 39-44 and 46-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh et al. (US 6625766) and Claims 22 and 45 are unpatentable over Oh et al. (US 6625766) in view of Giles et al. (US 6085334).

9. In reference to independent Claims 1, 39 and 44, rejected under 35 U.S.C. 103(a) as being unpatentable over Oh, the Applicant argues that it would not have been

obvious to modify Oh in a manner that would undermine Oh's clearly stated object and, therefore, that it would not have been obvious to modify Oh to achieve the above-recited combination.

Regarding independent Claims 1, 39, 44, the Examiner admitted that Oh does not disclose a second counter for incrementally adjusting the limit value in response to a second control signal. However, Oh substantially discloses an identical first counter circuit (address counter 44) coupled to the memory array (100) and a second counter circuit including an X-address maximum value register (42). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to add the identical address counter 44 between the register (42) and the comparison circuit 60, in the second counter circuit of Oh, as to incrementally adjust the limit value by increasing or decreasing the counter accordingly, in response to the second control signal (CLEAR), since the counter in the second counter circuit functions identically with the counter in the first counter circuit.

In response to applicant's argument that there is no suggestion to modify the Oh reference, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

In this case, Oh clearly discloses a second counter circuit including an X-address maximum value register (42), which upon comparison (50) with the first counter generates the second control signal (CLEAR), such as X carry out signal XCARRY, if the address value (44-OUT) and the limit value (42-OUT) have the same value, then XCARRY is logic "1". The modified reference of Oh meets the claimed invention, which recites in part

"A first counter circuit adapted to ....reset the address value to a start address in response to a second control signal", such as X carry out signal XCARRY.

"A second counter circuit to incrementally adjust the limit value in response to the second control signal" and

"A compare circuit coupled to receive the address value from the first counter circuit and the limit value from the second counter circuit, adapted to assert the second control signal if the address value and the limit value have a predetermined relationship", namely if the two counter values are the same, the compare circuit (60) receives the address value from the first counter circuit (44) and the limit value from the second counter circuit (42), and generates the second control signal (CLEAR) such as X carry out signal XCARRY, if the address value (44-OUT) and the limit value (42-OUT) have the same value, then XCARRY is logic "1".

In this case the XCARRY is being used a CLEAR signal for the first counter and as a CLOCK signal for the second counter.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
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Date: 15 November 2004
Office Action: Final Rejection

By: _____

JAMES C KERVEROS
Examiner
Art Unit 2133

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